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DESIGNING LOW POWER DOUBLE TAILED COMPARATOR FOR ECG

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Abstract: **While designing ECG systems, one of the chief issues is power consumption, most especially for mobile and wearable devices. This paper proposes the DTLC suitable for both low-end and high-end applications employing double-tailed comparators with negative body biasing to improve power throughout in ECG signal monitoring systems modeled using the Mentor Graphics. Integrated circuit designs with EDA tools using 180nm CMOS technology at a power supply of 0.8V improve power consumption without a decline in the car's performance. Parameters including power consumption and power-delay product (PDP) are improved with power dissipation reduced from 18.5 from 1.33 µW to 12.5 pW at a clock frequency of 20 kHz and the PDP reduced to 0.251 aJ at 27°C. These optimizations make the proposed comparator highly appropriate for low-power, high-performance ECG systems, especially in portable and wearable medical devices where power as resource utilization and accuracy in delivery are important factors. The design provides a sound platform for the analog to digital transition for the company. Analog-to-digital converters (ADCs) in cardiac signal monitoring as the customer requirement for energy-efficient acoustic elements in the medical industry grows. In this way, power release efficiency is improved, and excessive energy consumption is restrained. According to the accuracy requirements, the proposed comparator can be regarded as the most suitable for the modern ECG applications.**

Keywords: **ECG systems,Portable devices, Wearable technology, Double-tail latched comparator, Negative body biasing, Power efficiency, Power consumption, CMOS technology, Analog-to-digital converters (ADCs), Power dissipation,Power-delay product (PDP), Signal monitoring, Low-power design,Medicaldevices,Cardiacmonitoring,Energy-efficient components, Performance optimization, Simulation, Mentor Graphics EDA, Mentor Graphics EDA**

I. INTRODUCTION

The increasing popularity of wearable health devices has created a greater need for low-power ECG systems that can deliver reliable and continuous cardiac monitoring. A key challenge is to minimize power consumption while ensuring accuracy, which is vital for prolonging battery life in portable applications. Double-Tailed Latched Comparators (DTLCs) provide a promising solution, allowing for low-power, high-precision analog-to-digital conversion in ECG systems. This paper introduces an optimized DTLC, designed using Mentor Graphics EDA tools on 180nm CMOS technology and operating at 0.8V. This design significantly lowers power dissipation and enhances the power delay product (PDP), making it particularly well-suited for contemporary ECG devices. The optimized DTLC fulfills critical energy efficiency and accuracy standards, pushing forward the development of dependable, low-power ECG systems for portable medical use.

II. PROPOSED ALGORITHM

A. Initialization

The ECG signal monitoring set of rules begins with the initialization segment, wherein vital parameters are installed for filling performance. This consists of configuring the Analog-to-Digital Converter (ADC) parameters, which include sampling fee (generally around 250 Hz) and resolution (e.g., 12-bit), tailor-made to the precise requirements of the software. The double-tail latched comparator is then calibrated with suitable biasing settings to enhance its sensitivity and minimize energy consumption. Proper initialization is important to make certain that the subsequent processing and evaluation yield accurate and dependable ECG readings.

B. Signal Acquisition.

In the signal acquisition section, the device constantly monitors ECG indicators captured via electrodes placed at the affected person's pores and skin. These electrodes come across the electrical hobby of the coronary heart and relay the analog alerts to the comparator. The comparator digitizes those analog signals, converting them into a digital format that may be processed by using the machine. It is vital that this digitization procedure continues power dissipation in the targeted threshold (e.g., ≤ 12.wi-five pW) to make certain prolonged battery lifestyles in transportable gadgets. This segment is important for capturing real-time ECG facts necessary for correct monitoring.

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C. Information Processing

As soon as the ECG signals are digitized, the algorithm moves to the records processing segment. Here, digital wirelessltering techniques are carried out to enhance signal quality and reduce noise. Low-skip wireless filters are used to dispose of excessive-frequency interference, while notch wireless filters can wirelessly dispose of energy line noise (e.g., at 50/60 Hz).Subsequent, key functions from the ECG signal are extracted. The Pan-Tompkins set of rules is often hired to discover R-peaks, which can be essential for measuring coronary heart rate and identifying rhythmic styles. Additionally, wavelet rework strategies are utilized to come across QRS complexes, which might be indicative of heartbeats. Following characteristic extraction, heartbeat detection algorithms are applied. These may encompass thresholding techniques or systems gaining knowledge of strategies, along with guide vector machines or neural networks, to classify heartbeats accurately and identify ability anomalies, consisting of arrhythmias.

D. Power control

Powerful electricity management is vital in wearable or portable ECG tracking devices. The algorithm employs dynamic voltage and frequency scaling (DVFS), allowing the gadget to adjust its running situations primarily based on the contemporary workload. For example, while signal processing demands are low, the device can lessen voltage and frequency to preserve power. Moreover, power-saving modes are activated during idle intervals or levels of low pastime, extensively minimizing usual power consumption and increasing battery lifestyles. Records Transmission For fact transmission, the processed ECG facts are compressed to make sure efwireless transfer to far-flung servers or mobile devices. Compression algorithms, which include Huffman coding or wavelet compression, are employed to lessen the facts length whilst preserving critical sign records. This is mainly crucial in bandwidth-limited environments. The machine utilizes low-power verbal exchange protocols, which include Bluetooth Low electricity, to facilitate data transfer. Theseprotocols are optimized for minimal energy intake, permitting non-stop monitoring without rapidly depleting the tool's battery.

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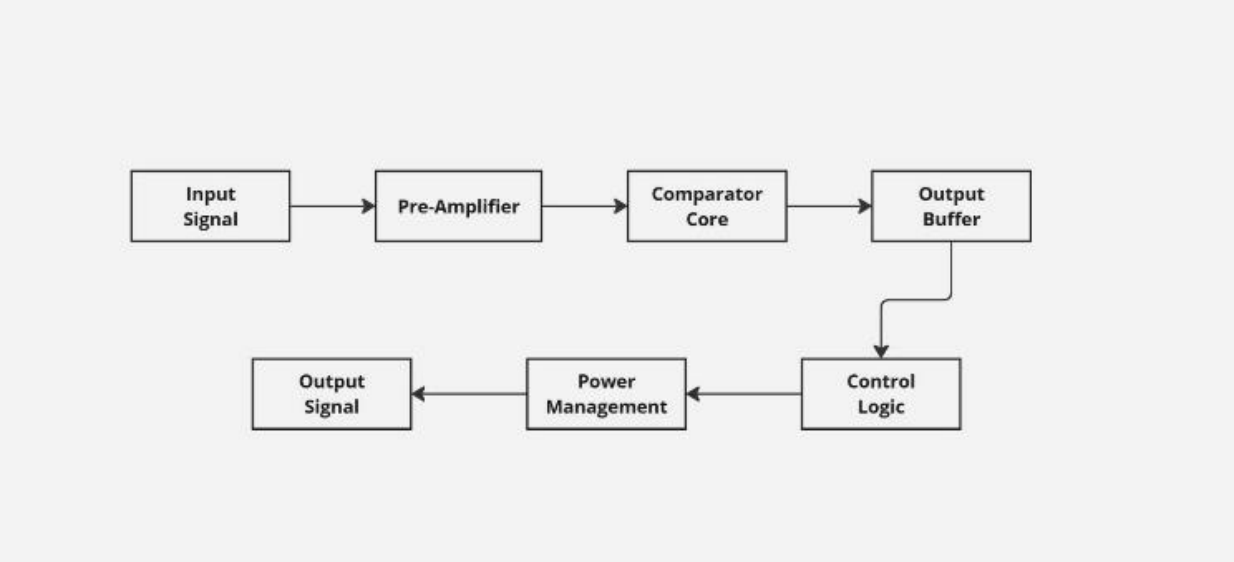

Fig.1. Block Diagram of Comparator

E. Person remarks and alerts

The system provides actual-time feedback to users based on the ECG readings. This comment may be visible, inclusive of showing heart rate or rhythm on a display, or auditory, using alerts or tones to signify precise heart situations. Additionally, a threshold-based totally alert device is implemented to inform users or healthcare vendors within the event of atypical readings or vital modiwireless in heart activity. This well-timed feedback is crucial for proactive fitness control. Non-stop getting to know and version subsequently, the set of rules incorporates non-stop learning and version abilities. Machine learning fashions are included in the gadget to rewire detection algorithms based totally on amassed information and person comments. As greater statistics are amassed, the device can improve its accuracy and reliability in detecting heart conditions. Furthermore, the machine dynamically updates its parameters to evolve to various physiological situations of the consumer, improving ordinary performance and personalizing the monitoring experience.

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III. EXPERIMENT AND RESULT

The proposed double-tail latched comparator was analyzed and tested in the current paper and the study through simulations with the help of Mentor Graphics EDA tools by utilizing 180nm CMOS technology on a supply voltage of 0.8V. The main goals were to evaluate power consumption, timing, as well as power versus delay. product defined as per predetermined product development process (PDP) at a clock frequency of 20 kHz.

A. Power Dissipation

The fact that the number of signals that have to be processed reduced and hence power dissipation was the biggest discovery made according to the study. The proposed comparator demonstrated a power consumption of 12.5 pW, which is 6 pW less than the 18.5 pW not seen in conventional comparator structures. This is about 32.4 percent lower than the number of results obtained when only 'technology' was entered into the search, which illustrates that negative body biasing is useful since it enhances the need for a reliablemethod of drop. When it comes to software, the developed theories promise to enhance power efficiency in portable ECG devices.

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B. Delay Analysis

It is worth understanding the delay effect while having an improvement in the power dissipation. The proposed design yielded a somewhat higher delay than the traditional comparators revealed. Still, there is a need to put specific delay values into play, such as boost, due to the added challenges that are normally associated with coming up with negative body biasing. However, the trade-off is justified with this kind of relationship being easier for couples already accustomed to one another and learning to adapt to changes after kids are born. Particularly for those low-power applications, where power usage is a critical factor in the design of the system.

C. Power-Delay Product (PDP)

The productivity- delay index can be defined as the overall index of efficiency. The PDP for the proposed comparator was calculated to be 0.251aJ, this was even better than the previous conventional design. This decline in PDP underlines the viability of the proposed comparator to give good performance with lower energy consumption and therefore ideal for systems that require a significant power consumption, and at the same time high precision

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D. Circuit Waveform Analysis

They generated important waveform displays that show the workings of the proposed comparator.

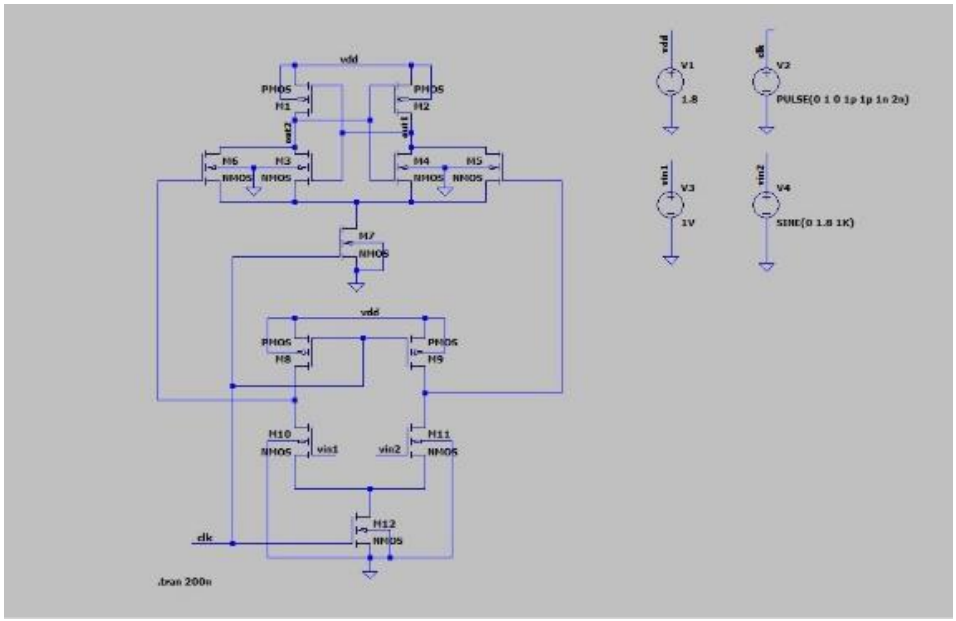

Fig.2. Double Tail Latched Comparator

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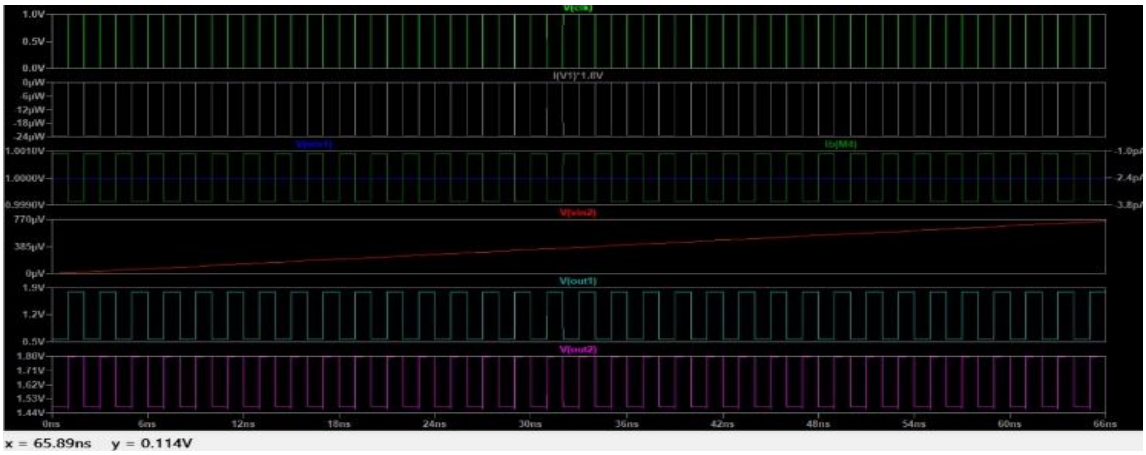

Fig.3. double tail latched comparator output waveform

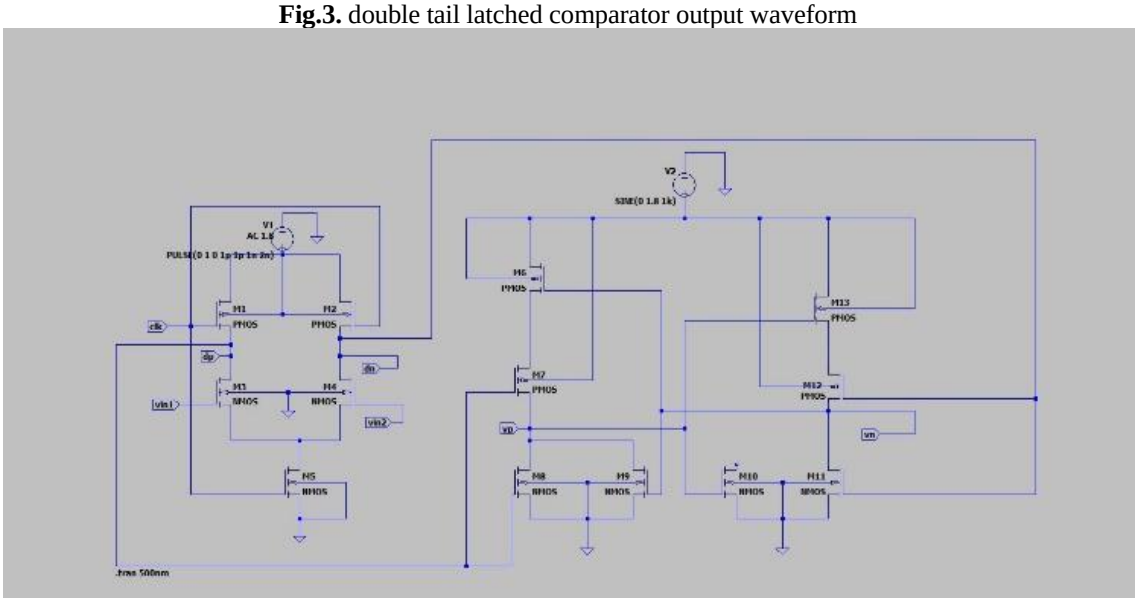

Fig.4. SR Latched dynamic comparator circuit

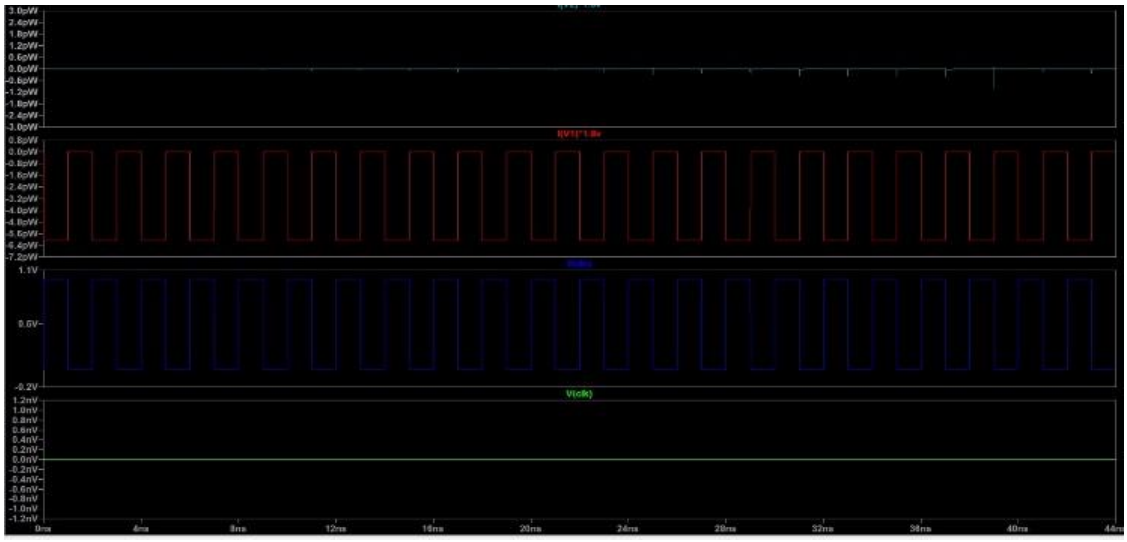

Fig.5.SR Latched dynamic comparator circuit output waveform

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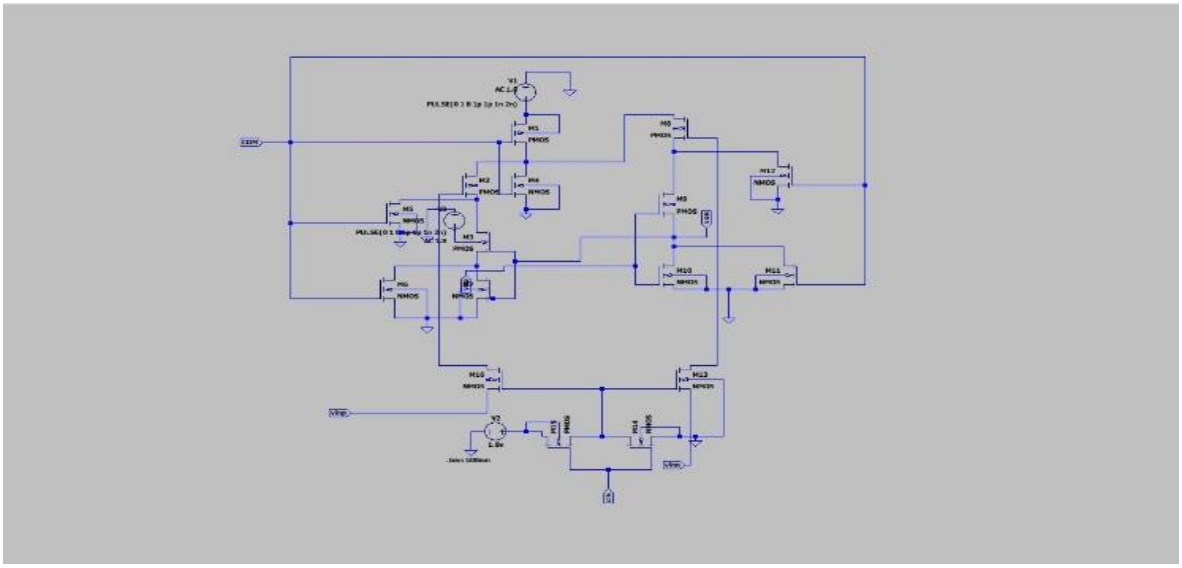

Fig.6. Single tail latched comparator circuit

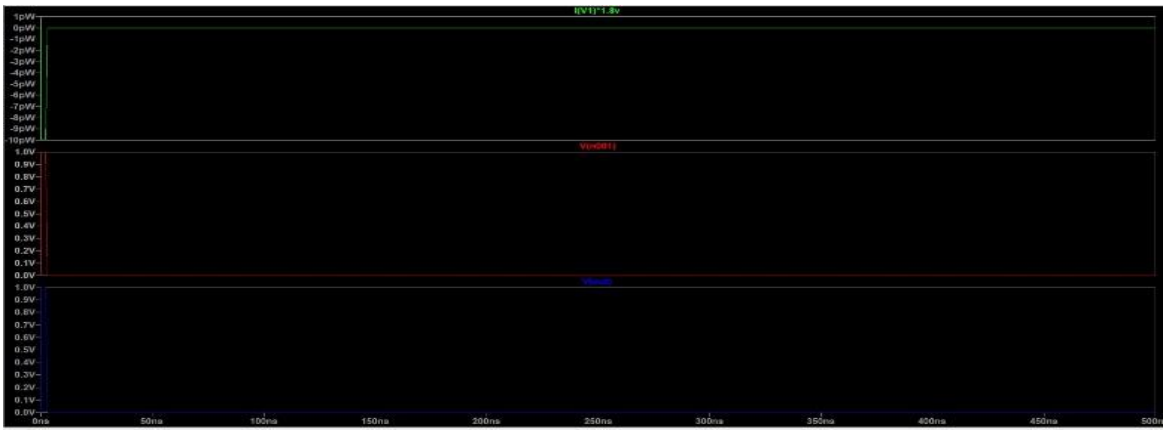

Fig.7. Single tail latched comparator circuit output waveform

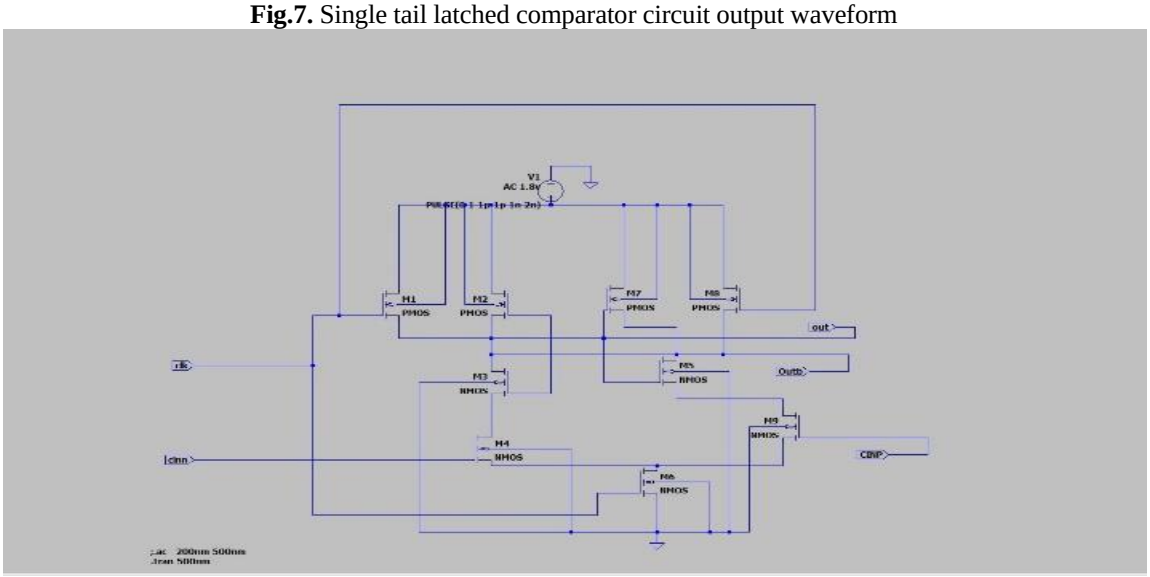

Fig.8. Latched regenerative comparator circuit

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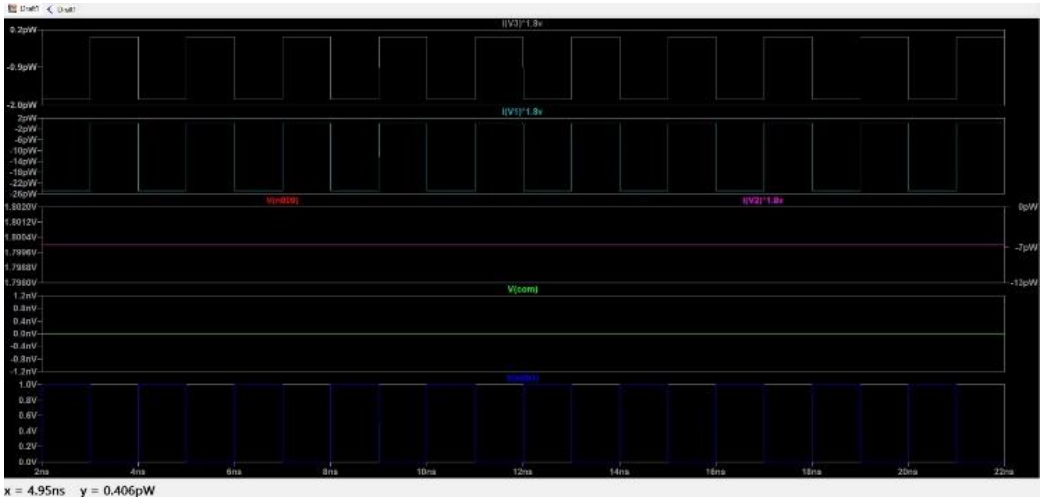

Fig.9. Latched regenerative comparator circuit output waveform

E. Comparative Evaluation

While comparing the proposed double-tail latched comparator with the existing designs, it is evident that negative body biasing leads to improved overall efficiency of the device. The reduction in both power dissipation and PDP places the comparator in a good standing for the next stage. Mainly for low-powered ECG monitoring applications, where energy consumption is of paramount importance.

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F. Further meanings regarding ECG technology

These findings have great implications for the production of portable and wearable devices. ECG devices, through the increased efficiency in the use of power as has been demonstrated above, will be able to attain optimum performance without necessarily recording increased demands on power. The proposed design satisfies the new emerging market need for energy-efficient medical equipment.

SL. NO.	Year	Authors	Focus of the paper	Key points in coverage	Technique used	Parameters Analyzed	Research Gaps
1	2022	Weijian Chen, Yanhan Zeng, Zhixian Li, Jingci Yang and Yongfu Li	Low-power ECG ADC	Energy-efficient ADC	Body-driven biasing technique	Power consumption,resolution, noise	Scalability, integration, noise
2	2020	N. Singh and M. Kumar	Power optimization, ADC	Comparator design, simulation	Negative body biasing	Power consumption,performance,delay	Robustness, integration, technology
3	2018	Bala Dastagiri,Kakarla Hari Kishore,Vinit Kumar Gunjan and Shaik Fahimuddin	Dynamic comparator design	Power efficiency, noise reduction	Dynamic latched comparator	Power dissipation, kickback noise, resolution	Scalability, integration, testing
4	2016	N.Bala Dastagiri and K.Hari Kishore	Power, noise trade-off	Trade-offs, designs,applications	Dynamic comparator design	Power dissipation, kickback noise	Optimization, implementation, integration

Fig.10. Comparison of Literature survey

IV. CONCLUSION

The proposed double-tail latched comparator, featuring negative body biasing, offers substantial gains in energy efficiency, positioning it as an ideal solution for low-power ECG monitoring. Simulations using Mentor Pix EDA tools and 180nm CMOS technology highlight a remarkable power dissipation reduction—from 18.5 pW to 12.5 pW—representing a 32.4% decrease while upholding system performance at a 20 kHz clock frequency. Although implementing negative body biasing introduces a minor delay, this is a reasonable trade-off in the context of low-power designs focused on energy savings. The energy-delay product (PDP) of 0.251 aJ further underscores the comparator's efficiency, making it highly suitable for high-performance applications. Comparisons with existing designs reveal that

innovative methods like negative body biasing not only improve energy efficiency but also enhance the device's viability for integration in portable and wearable ECG systems. Additionally, this study aligns with the medical technology trend towards minimizing energy consumption and maintaining precision, addressing challenges related to noise management and optimizing trade-offs between power and performance. This work contributes to the field of power-efficient medical devices, meeting the increasing need for reliable ECG monitoring in portable applications and offering a promising pathway for future analog-to-digital converters in healthcare technology.

V. REFERENCES

[1] Dastagiri, Bala & Kakarla, Hari & Gunjan, Vinit & Shaik, Dr. Fahimuddin. (2018). Design of a Low-Power Low-Kickback-Noise Latched Dynamic Comparator for Cardiac Implantable Medical Device Applications. DOI:10.1007/978-981-10-4280-5_67

[2] Pradeep, Jinka & Ramashri, T. (2023). Design of low power dynamic comparator with reduced kickback noise technique for bio-medical applications. e-Prime - Advances in Electrical Engineering, Electronics and Energy. DOI: 6. 100336. 10.1016/j.prime.2023.100336.

[3] Singh, Neha & Kumar, Manish. (2020). Low Power CMOS Negative Body Biased Double-tail Latched Comparator for ECG Applications. DOI:538-540. 10.1109/ICE348803.2020.9122840.

[4] Dastagiri, Bala & Kakarla, Hari & Gunjan, Vinit & Shaik, Dr. Fahimuddin. (2018). Design of a Low-Power Low-Kickback-Noise Latched Dynamic Comparator for Cardiac Implantable Medical Device Applications. DOI: 10.1007/978-981-10-4280-5_67.

[5] M. S. Babayan-Mashhadi and R. Lotfi,(2014) "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 22, no. 2, pp. 343-352, DOI: 10.1109/TVLSI.2013.2241799.

[6] S. S. Baghel and D. K. Mishra,(2018) "Design and Analysis of Double-Tail Dynamic Comparator for Flash ADCs," International Conference on Circuits and Systems in Digital Enterprise Technology (ICCSDET), Kottayam,India,pp.1DOI:10.1109/ICCSDET.2018.882112

[7] A. Kannaujiya, S. Kannaujiya and R. K. Chauhan, "Effect of Gate Metal Work Function on Leakage Current in Single Pocket FDSOI 28 nm Transistor," 2021 10th IEEE International Conference on Communication Systems and Network Technologies (CSNT), Bhopal, India, 2021, pp. 241-246, doi: 10.1109/CSNT51715.2021.9509715..

[8] P. M. Figueiredo and J. C. Vital,(2016) "Kickback noise reduction techniques for CMOS latched comparators," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 53, no. 7, pp. 541-545, doi: 10.1109/TCSII.2006.875308.

[9] S.Y. Peng, L.H. Liu, P.K. Chang, T.Y. Wang, H.Y. Li,(2017) A power-efficient reconfigurable output-capacitor-less low-drop-out regulator for low-power analog sensing front-end, IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. 64 (6) 1318–1327.

[10] Heung Jun Jeon and Yong-Bin Kim,(2012) "A novel low power lowoffset and high speed CMOS dynamic latched comparator,"Analog Integrated Circuits and Signal Processing, pp.70:337-346.

[11] Chandrakasan AP, Verma N, Daly DC,(2018) Ultralow- Power Electronics for Biomedical Applications, Annual Review of Biomedical Engineering; 10:247−74.

[12] Zhang D, Bhide A, Alvandpour A,(2012) A 53-nW 9.1-ENOB 1-KS/s SAR ADC in 0.13um CMOS for Medical Implant Devices, IEEE Journal of Solid State Circuits. 47(7):1588−93.

[13] Anantha P. Chandrakasan, Naveen Verma and Denis C. Daly,(2008) "Ultralow- Power Electronicsfor Biomedical Applications" Annu. Rev. Biomed. Engg.

[14] W. H.Maisel, M. O. Sweeney, W. G. Stevenson, K. Ellison, and L. M. Epstein,(2001) BRecalls andsafety alerts involving pacemakers and implantable cardioverter-defibrillator generators, J. Amer. Med. Assoc., vol. 286, pp. 793–799.